WHAT IS CLAIMED IS:

1. A magnetic memory device comprising:

first to n-th MTJ devices recording data;

first to n-th transistors connected to the first to n-th MTJ devices, respectively;

a write word line which generates a magnetic field to be applied to the first to n-th MTJ devices during a write operation;

a read word line which is connected to a gate of each of the first to n-th transistors and which applies a voltage for turning on the first to n-th transistors during a read operation;

a first word line driver which is connected to a first end or a second end of the write word line and which drives the write word line;

a second word line driver which is connected to a first end of the read word line and which drives the read word line; and

a second switching circuit which selectively connects a second end of the read word line and the second end of the write word line.

2. The device according to claim 1, wherein the second switching circuit is constituted by a P-type MIS transistor.

3. The device according to claim 1, wherein the second switching circuit is constituted by an N-type MIS transistor.

4. The device according to claim 2, wherein the second switching circuit further comprises an N-type MIS transistor which is connected in parallel to the P-type MIS transistor.

5. The device according to claim 1, further comprising a first switching circuit which selectively connects the first end of the read word line and the first end of the write word line.

6. The device according to claim 5, wherein each of the first and second switching circuits is constituted by a P-type MIS transistor.

7. The device according to claim 5, wherein each of the first and second switching circuits is constituted by an N-type MIS transistor.

8. The device according to claim 6, wherein each of the first and second switching circuits further comprises an N type MIS transistor, which is connected in parallel to the P-type MIS transistor.

9. The device according to claim 6, wherein the first switching circuit acts as the second word line driver to which power is supplied via the write word line.

10. The device according to claim 9, further comprising a first clamp circuit which is connected between the first end of the read word line and a first wiring.

11. The device according to claim 10, wherein the

first clamp circuit is constituted by an N-type MIS transistor.

12. The device according to claim 11, wherein the potential of the first wiring is ground potential.

13. The device according to claim 10, further comprising a fourth word line driver which drives the write word line and which is connected in parallel to the first word line driver.

14. The device according to claim 13, wherein the first word line driver has a current driving ability larger than the fourth word line driver.

15. The device according to claim 9, wherein the second switching circuit acts as a third word line driver which drives the read word line and to which power is supplied via the write word line.

16. The device according to claim 15, further comprising a second clamp circuit which is connected between the second end of the read line and the first wiring.

17. The device according to claim 16, wherein the second clamp circuit is constituted by an N-type MIS transistor.

18. The device according to claim 15, further comprising a fourth word line driver which drives the write word line and which is connected in parallel to the first word line driver.

19. The device according to claim 18, wherein the

first word line driver has a current driving ability larger than the fourth word line driver.

20. The device according to claim 1, further comprising a current sinker which is connected to one of the first end and the second end of the write word line, to which the first word line driver is not connected, and which acts for drawing out the current flowing through the write word line.

21. The device according to claim 1, wherein the write word line intersects successively with the first to n-th MTJ devices from the first end to the second end; and the read word line intersects successively with the gates of the first to n-th transistors from the first end to the second end.

22. The device according to claim 1, wherein the first to n-th MTJ devices form a memory cell row, which is arranged in a single memory cell array.

23. The device according to claim 1, wherein the first to n-th MTJ devices form a memory cell row and the memory cell row is arranged repeatedly a plurality of times to form a plurality of memory cell arrays.

24. A magnetic memory device comprising:

first to n-th MTJ devices recording data;

first to n-th transistors connected to the first to n-th MTJ devices, respectively;

a write word line which generates a magnetic field to be applied to the first to n-th MTJ devices during

a write operation;

a read word line which is connected to a gate of each of the first to n-th transistors and which applies a voltage for turning on the first to n-th transistors during a read operation;

a first word line driver which is connected to a first or a second end of the write word line and which drives the write word line;

a first switching circuit which selectively connects the first end of the write word line and the first end of the read word line; and

a second switching circuit which selectively connects the second end of the write word line and the second end of the read word line.

25. The device according to claim 24, further comprising a fourth word line driver which drives the write word line and which is connected in parallel to the first word line driver.

26. The device according to claim 25, wherein the first word line driver has a current driving ability larger than the fourth word line driver.

27. The device according to claim 24, further comprising a current sinker which is connected to one of the first end and the second end of the write word line, to which the first word line driver is not connected, and which acts for drawing out the current flowing through the write word line.

28. The device according to claim 24, wherein the write word line intersects successively with the first to n-th MTJ devices from the first end to the second end; and the read word line intersects successively with the gates of the first to n-th transistors from the first end to the second end.

29. The device according to claim 24, wherein the first to n-th MTJ devices form a memory cell row, which is arranged in a single memory cell array.

30. The device according to claim 24, wherein the first to n-th MTJ devices form a memory cell row and the memory cell row is arranged repeatedly a plurality of times to form a plurality of memory cell arrays.